LH51256

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time: 100 ns (MAX.)
- Power consumption:
  - Operating: 275 mW (MAX.)
    (T_A = -40 to 85°C, minimum cycle)
  - Standby:
    27.5 µW (MAX.) (T_A = -40 to 85°C)
    5.5 µW (MAX.) (T_A = 0 to 60°C)
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  - 28-pin, 600-mil DIP
  - 28-pin, 450-mil SOP

DESCRIPTION

The LH51256 is a 256K bit static RAM organized as 32,768 × 8 bits which provides low-power standby mode. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

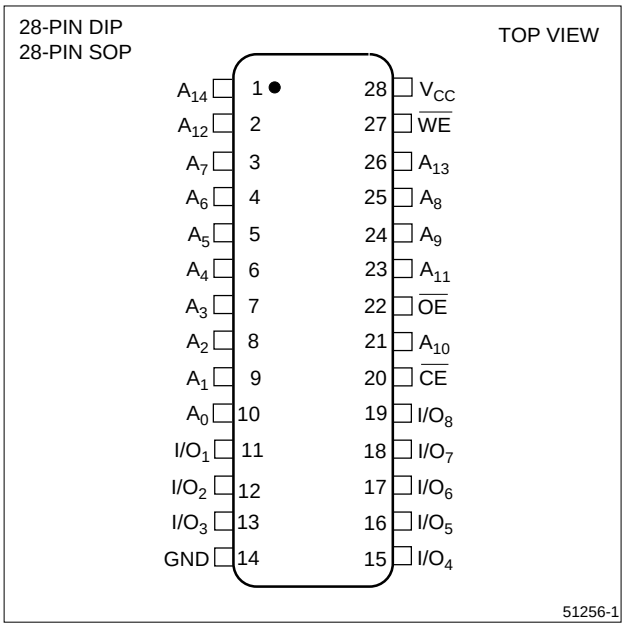


Figure 1. Pin Connections for DIP and SOP Packages

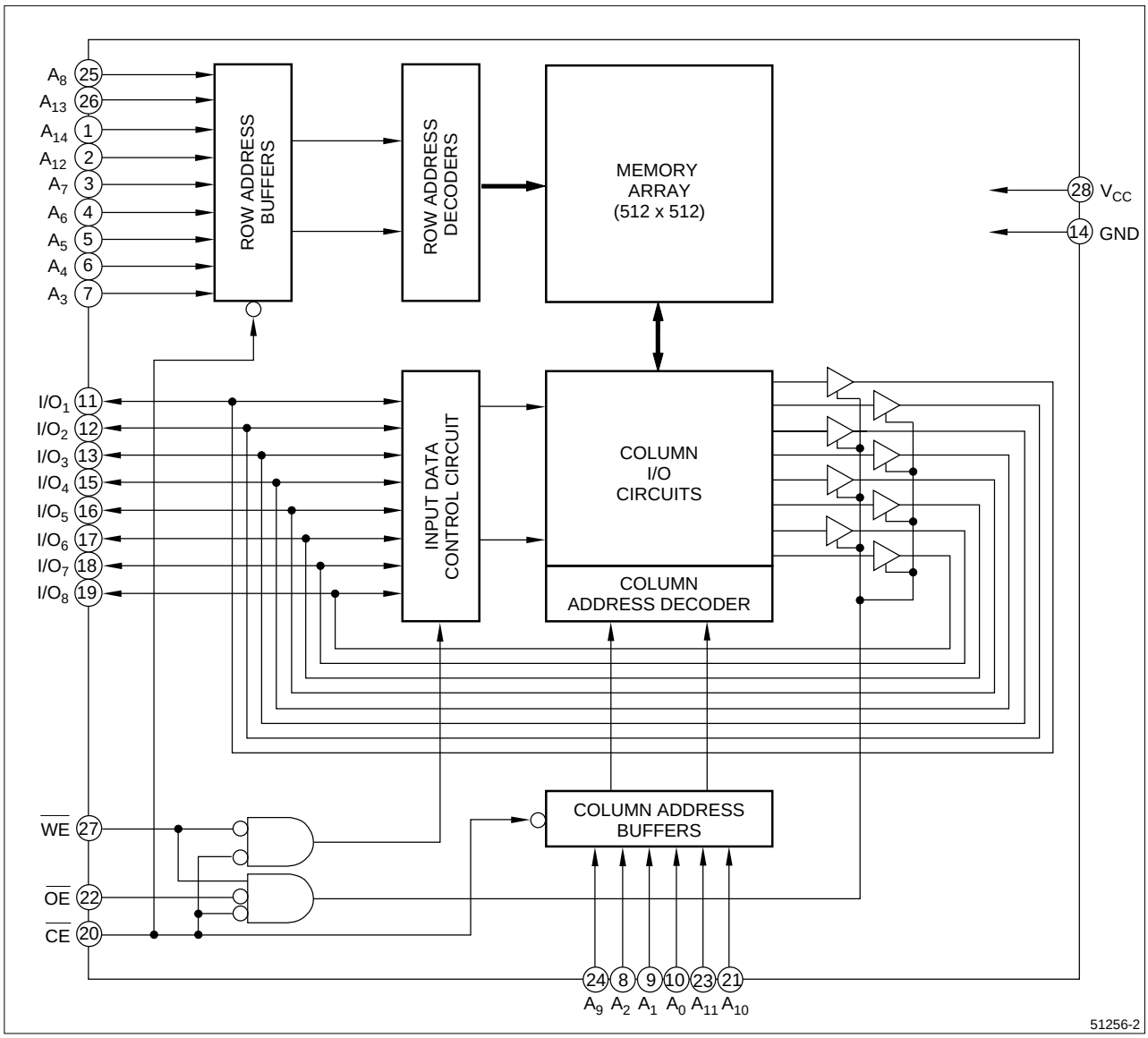


Figure 2. LH51256 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address input
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1, 2
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. V_{IN} (MIN.) = -3.0 V for pulse width ≤50 ns.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V	
	V_{IL}	-0.3		0.8	V	1

NOTE:
1. V_{IL} (MIN.) = -3.0 V for pulse width ≤50 ns.

DC CHARACTERISTICS (V_{CC} = 5 V ±10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	V_{CC} = 5.5 V V_{IN} = 0 to V_{CC}	-1		1	µA
Output leakage current	I_{LO}	$\overline{CE}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}	-1		1	µA
Operating current	I_{CC}	$\overline{CE}$ = V_{IL}, Outputs open			50	mA
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			10	mA
	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V T_A = 0 to +60°C			1	µA
		$\overline{CE}$ ≥ V_{CC} - 0.2 V T_A = -40 to +85°C			5	µA
Output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ±10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100		ns	
Address access time	t_{AA}		100	ns	
Chip enable access time	t_{ACE}		100	ns	
Output enable access time	t_{OE}		50	ns	
Output hold time	t_{OH}	5		ns	
$\overline{CE}$ Low to output in Low-Z	t_{LZ}	5		ns	1
$\overline{OE}$ Low to output in Low-Z	t_{OLZ}	5		ns	1
$\overline{CE}$ High to output in High-Z	t_{HZ}	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	ns	1

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

(2) WRITE CYCLE (V_{CC} = 5 V ±10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100		ns	
$\overline{CE}$ Low to end of write	t_{CW}	90		ns	
Address valid to end of write	t_{AW}	90		ns	
Address setup time	t_{AS}	0		ns	
Write recovery time	t_{WR}	0		ns	
Write pulse width	t_{WP}	50		ns	
Input data setup time	t_{DW}	30		ns	
Input data hold time	t_{DH}	0		ns	
$\overline{WE}$ High to output in High-Z	t_{OW}	0		ns	1
$\overline{WE}$ Low to output in High-Z	t_{WZ}	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	ns	1

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±200 mV transition from steady state levels into the test load.

AC TEST CONDITIONS

PARAMETER	MODE	NOTE
Input voltage amplitude	0.6 to 2.4 V	
Input rise/fall time	10 ns	
Timing reference level	1.5 V	
Output load conditions	1TTL + C_L (100 pF)	1

NOTE:
1. Includes scope and jig capacitance.

CAPACITANCE [1] (T_A = 25°C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V		2.0	5.5	V	
Data retention current	I_{CCDR}	V_{CCDR} = 3.0 V, $\overline{CE} \geq V_{CCDR}$ - 0.2 V	T_A = 25°C		0.2	µA	
			T_A = 0 to 60°C		0.6		
					3.0		
$\overline{CE}$ setup time	t_{CDR}			0		ns	
$\overline{CE}$ hold time	t_R			t_{RC}		ns	1

NOTE:
1. t_{RC} = Read cycle time

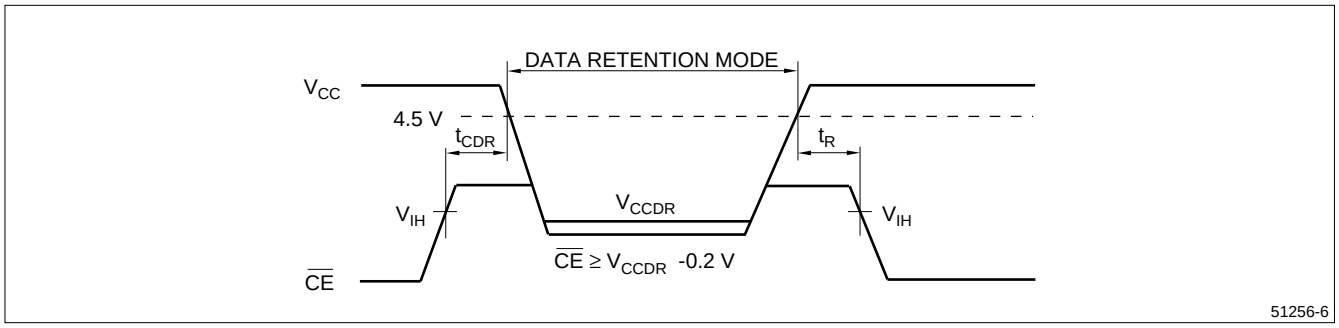


Figure 3. Data Retention Characteristics

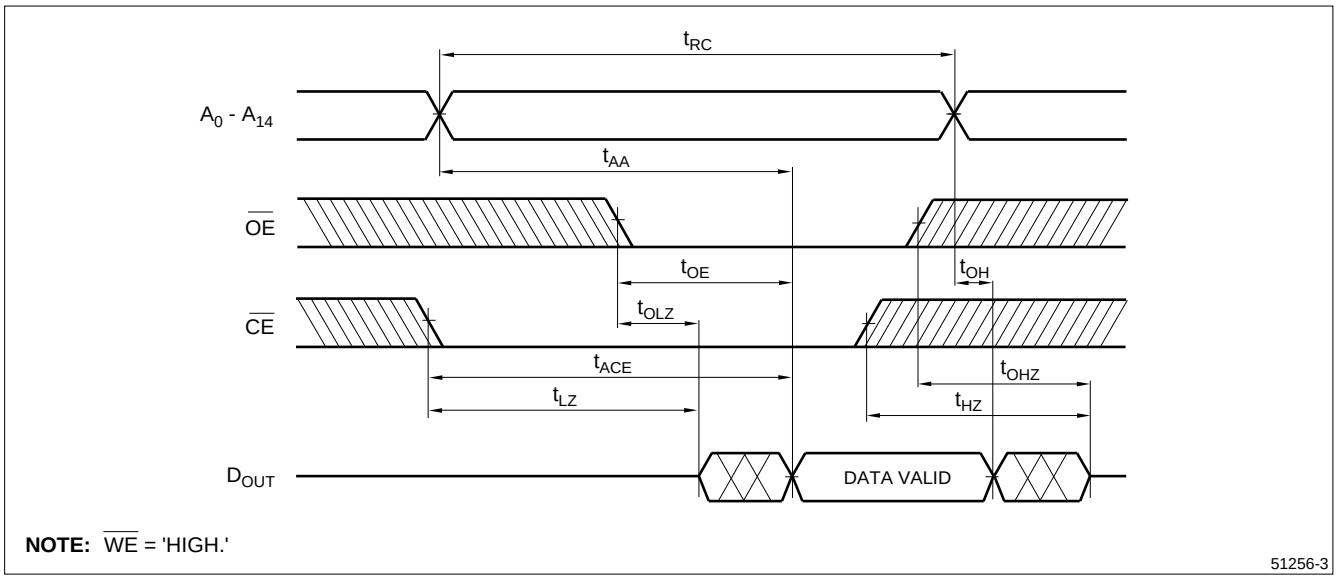
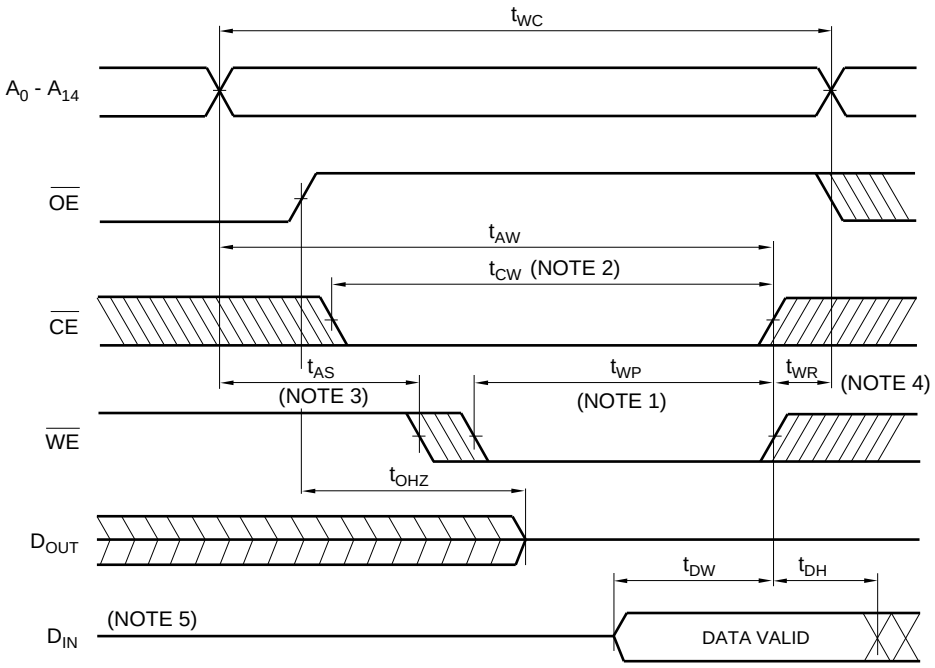


Figure 4. Read Cycle



NOTES:

1. The writing occurs during an overlapping period of $\overline{CE}$ = 'LOW' and $\overline{WE}$ = 'LOW' (t_{WP}).
2. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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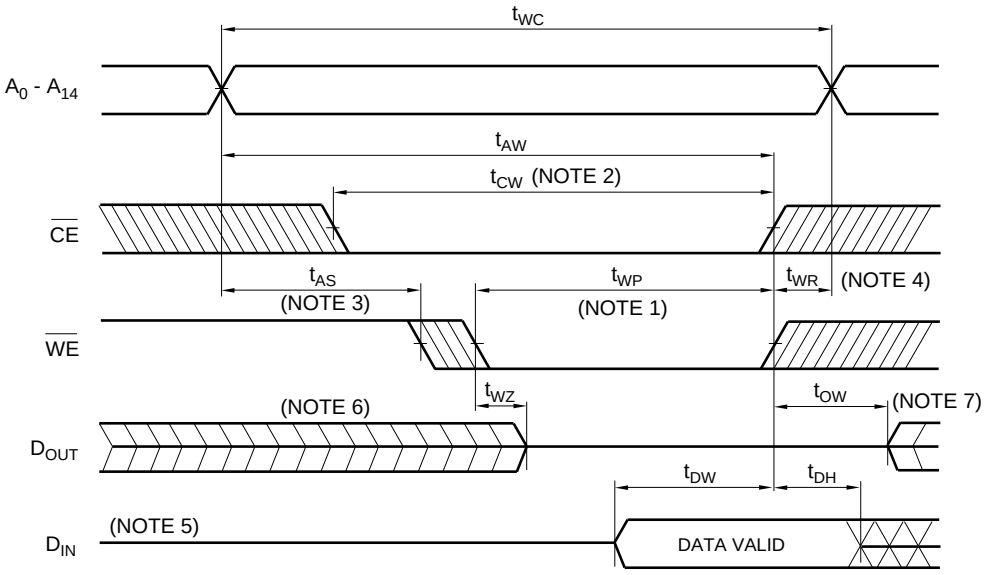
Figure 5. Write Cycle 1 ($\overline{OE}$ Clock)



NOTES:

1. The writing occurs during an overlapping period of $\overline{CE}$ = 'LOW' and $\overline{WE}$ = 'LOW' (t_{WP}).
2. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to address change.
5. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
7. If $\overline{CE}$ HIGH transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.

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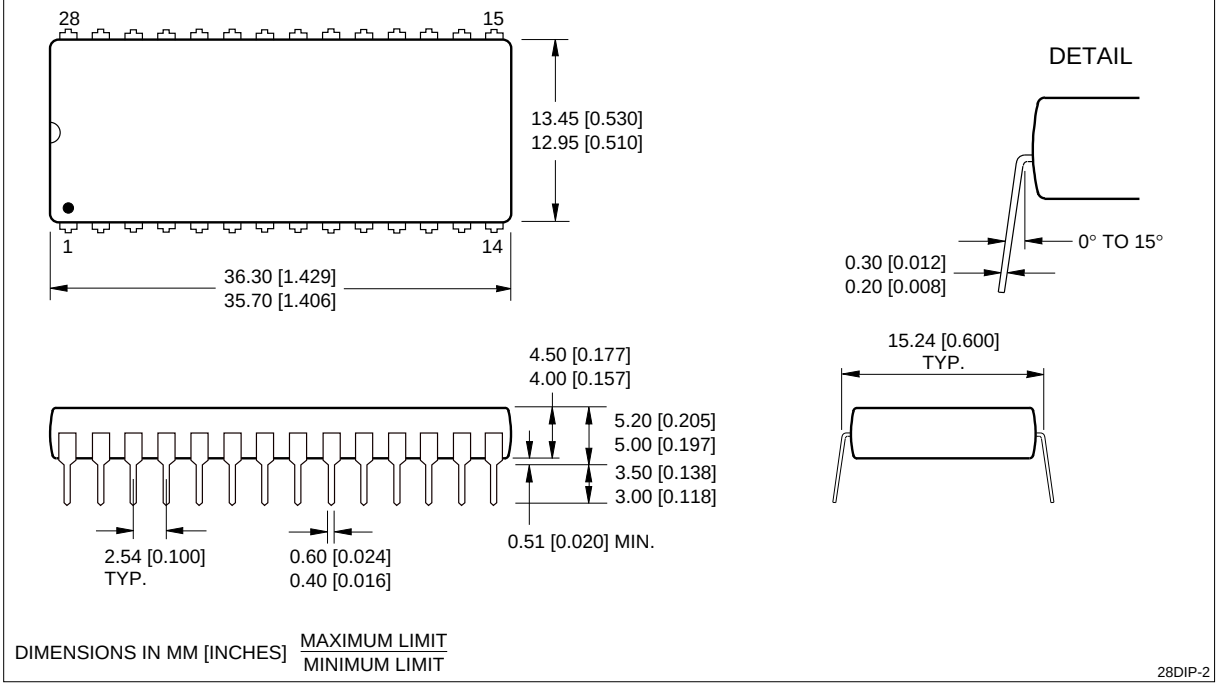
Figure 6. Write Cycle 2 ($\overline{OE}$ Low)

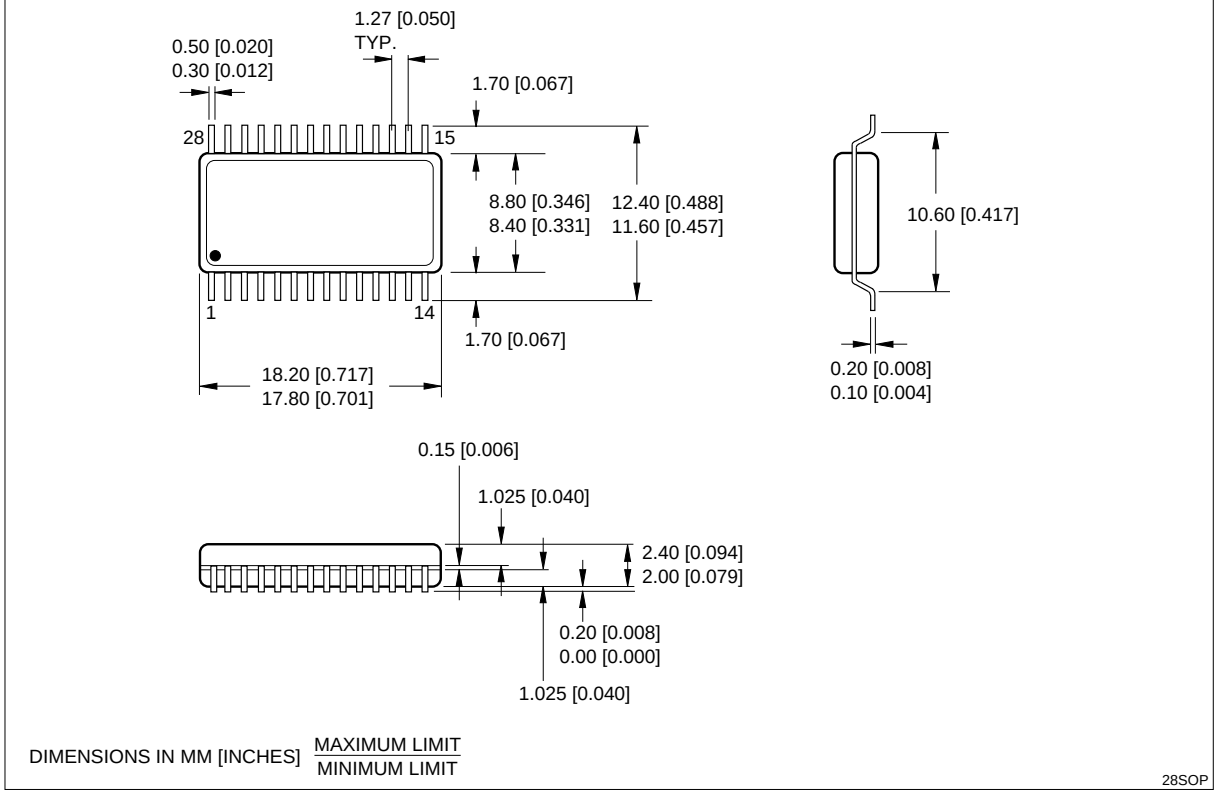
PACKAGE DIAGRAMS

28DIP (DIP028-P-0600)



28-pin, 600-mil DIP

28SOP (SOP028-P-0450)



28-pin, 450-mil SOP

ORDERING INFORMATION